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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/542,473	04/04/2000	Takayuki Ikeda	0756-2138	6069

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NIXON PEABODY, LLP
8180 GREENSBORO DRIVE
SUITE 800
MCLEAN, VA 22102

EXAMINER
SEFER, AHMED N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/542,473	IKEDA ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-10,16-33 and 35-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16-20,26-33 and 35-42* is/are allowed.

6)☒ Claim(s) *3-10 and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on 2/26/03 has been entered; no new claims have been added. And the indicated allowability of claims 3, 5-7, 24 and 25 is withdrawn in view of the newly discovered reference(s) to Yamazaki et al. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 3, 4, 6-9 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumoto US Patent No. 5,323,042 in view of Ikeda (JP 7-326767) and Otani (JP 10-56184).

Matsumoto discloses in fig. 1 a display device comprising a pixel portion 12 and a driver portion 13 on a substrate 11, said pixel portion comprising a semiconductor film comprising a channel forming region 21a, a plurality of impurity regions 21b, a source region 21c, and a drain region 21c; and a gate electrode 25 overlapping/partially overlapping with the channel forming region and some of the impurity regions, with a gate insulating film 24 interposed therebetween, wherein a gate insulating film of a TFT in said driver circuit portion and a dielectric of a storage capacitor formed in said pixel portion comprise the same material and have the same film

thickness, but omits a gate electrode overlapping plurality of channel regions and a thicker gate film in a pixel portion than one in a driver circuit portion.

Ikeda discloses in figs. 1-3 a plurality of channel regions 21 and a plurality of impurity regions 31A-C having the same conductivity type as a source 23 and drain 25 regions (as in claim 23) wherein some of the impurity regions are located between the plurality of the channel regions in the semiconductor film; and a gate electrode 14 overlapping with the channel forming regions and some of the impurity regions with a gate insulating film 13 interposed therebetween.

Otani discloses a thickness of a gate insulating film of a TFT in a driver circuit portion 20a; 20b is thinner than a gate insulating film of a TFT in a pixel portion 20c.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Ikeda with Matsumoto's device, since that would provide a pixel with a larger numerical aperture. It would have been obvious to incorporate the teachings of Otani, since that would execute a high-speed operation and reduce power consumption as taught by otani.

As to claims 6, 8 and 24, Ikeda discloses in fig. 3 a plurality of impurity regions 31 comprising a low concentration regions, a high concentration region, and wherein said some of the low concentration impurity regions and the high concentration impurity region are located between the plurality of the channel regions in the semiconductor film or the high concentration impurity region are located between a pair of low impurity regions under the gate electrode (as in claim 24).

As to claims 7, 9, 21-23 and 25, the prior art discloses at least two impurity regions overlapped with the gate electrode and at least one impurity region overlapped with the gate

electrode containing an element belonging to group XV in the periodic table (as in claims 22 and 25) but does not specifically disclose having a concentration as recited in the claim. However, it would have been obvious to optimize the device by using a workable range, which involves only a routine skill in the art. Further, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

4. Claims 4-6, 8, 10 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo US Patent No. 6,140,162 in view of Ikeda (JP 7-326767) and Otani (JP 10-56184).

Yeo discloses in fig. 3 a display device comprising a pixel portion and a driver portion on a substrate 200, said pixel portion comprising a semiconductor film comprising a channel forming region 41C, a plurality of impurity regions 41L, a source region 41S, and a drain region 41D; and a gate electrode 43G overlapping with the channel forming region, with a gate insulating film 42T interposed therebetween, wherein a gate insulating film 52 of a TFT in said driver circuit portion and a dielectric 42T of a storage capacitor formed in said pixel portion comprise the same material and have the same film thickness, but omits a gate electrode overlapping plurality of channel regions and a thicker gate film in a pixel portion than one in a driver circuit portion.

Ikeda discloses in figs. 1-3 a plurality of channel regions 21 and a plurality of impurity regions 31A-C having the same conductivity type as a source 23 and drain 25 regions (as in claim 23) wherein some of the impurity regions are located between the plurality of the channel

regions in the semiconductor film; and a gate electrode 14 overlapping with the channel forming regions and some of the impurity regions with a gate insulating film 13 interposed therebetween.

Otani discloses a thickness of a gate insulating film of a TFT in a driver circuit portion 20a; 20b is thinner than a gate insulating film of a TFT in a pixel portion 20c.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teaching of Ikeda with Matsumoto's device, since that would provide a pixel with a larger numerical aperture. It would have been obvious to incorporate the teachings of Otani, since that would execute a high speed operation and reduce power consumption as taught by otani.

As to claims 6 and 8, Ikeda discloses in fig. 3 a plurality of impurity regions 31 comprising a low concentration regions, a high concentration region, and wherein said some of the low concentration impurity regions and the high concentration impurity region are located between the plurality of the channel regions in the semiconductor film.

As for claims 5 and 10, the prior art omits that electronic equipment selected from the group consisting of a video camera, a digital camera and other various electronic equipment. However, Examiner takes Official Notice that an electronic equipment comprising a display device wherein said electronic equipment selected from the group consisting of a video camera or a digital camera is conventional and well known. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to have used any of the various electronic equipment since Examiner takes Official Notice that due to their low power consumption, displays have become a necessary and indispensable structural element of an electronic equipment.

Allowable Subject Matter

5. Claims 16-20, 26-33 and 35-42 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to disclose a device structure as recited in claims 16, 18 and 35.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yamazaki et al. US ref. 6,278,131 disclose a pixel TFT having a driver circuit portion with thinner gate oxide than the one of a pixel portion.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601.

ANS
May 19, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800